REMARKS

Claims 1-2, 5-15, and 19-22 are pending in the application. Claims 3, 4, and 16-18 have been canceled. Of these, claims 1, 15, and 20 are independent. Favorable consideration and examination are respectfully requested.

In the office action of October 17, 2005, claims 1-2, 5-8, and 20-22 were rejected under 35 U.S.C. 103(a) over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202). Claims 15-17, and 19 were rejected under 35 U.S.C. 102(e) over Boyd et al (US 2002/0028555). Claim 9 was rejected under 35 U.S.C. 103(a) over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202) and further in view of Buynoski (US 6,194,299).

Initially, Applicants thank the Examiner for indicating that claims 10-14 contain allowable subject matter and would be in condition for allowance if rewritten in independent form to include all the limitations of their base claims. Applicants, however, have not amended those claims, as suggested by the Examiner, because Applicants believe that all of the claims, as amended, are allowable for at least the reasons set forth below.

Independent claim 1 defines a method of fabricating a semiconductor structure. The method includes selecting chemical mechanical polishing parameters to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate.

On page 4 of the Office Action, the Examiner acknowledges that "Boyd fails to specifically disclose selecting chemical mechanical polishing parameters to remove the silicide

layer at a higher rate than the polysilicon." The Examiner relies on Thomas to teach this missing feature. In particular, the Examiner states on page 4 of the Office Action that:

> Thomas, in a method for controlling of removal rate in CMP, discloses that the difference in removal rate is characterized by a parameter termed the selectivity ratio (col 1, paragraph 0005)
> Since Boyd discloses removing a portion of the silicide laver [sic] 36 at a higher rate than polysilicon during the CMP process, one skilled in the art at the time the invention was made would have found it obvious to modify Boyd CMP process by selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate that the polysilicon as per Thomas because Thomas discloses that it is desirable for the removal rate of each layer to differ significantly from each other in order to reduce planarality ...

Applicants submit that neither Boyd nor Thomas, whether taken separately or in combination, disclose or suggest the features of claim 1, particularly with respect to selecting chemical mechanical polishing parameters to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate.

Applicants disagree with the Examiner's assertion on pages 4 and 6 of the Office Action that Boyd, in paragraph 72, discloses removing a portion of the silicide layer at a higher rate than polysilicon during the CMP process. In this regard, in paragraphs 72-73, Boyd states:

> [0072] After forming the insulator layer over the structure, any conventional planarization process such as chemical-mechanical polishing or grinding may be employed. It is noted that the planarization process employed in this step of the present invention is stopped after the silicide region 36 formed on top of polysilicon layer 52 is removed. Thus, the planarization exposes polysilicon layer 52 of the dummy gate region. The structure formed after conducting the above planarization step is shown in FIG. 2D.
> [0073] Next, polysilicon layer 52 is removed utilizing RIE or a chemical down stream etching process exposing pad oxide layer 14.

There is nothing in this passage that discloses or suggests that the rate at which the chemical-mechanical polishing (CMP) removes the silicide is higher than the rate at which the RIE or chemical etching process removes the polysilicon layer.

Applicants also disagree with the statement on page 6 of the Office Action that FIG. 2D of Boyd teaches the silicide layer having a higher removal rate than the polysilicon layer by showing "that all of the silicide layer 36 in the high region is removed after the CMP process while a portion of the polysilicon layer 52 still remains." The structure depicted in FIG. 2D in no way whatsoever supports the assertion that the silicide layer is removed at a higher rate than the polysilicon layer. The Examiner has misconstrued the order of removal of the silicide and polysilicon layers to be the rates of removal. In this regard, the structure depicted in FIG. 2D is simply an intermediate structure that is formed after the silicide layer is removed but before the polysilicon layer 52 is etched away. The foregoing passage clearly discloses that the polysilicon layer is removed after the silicide layer is removed. There is nothing in the foregoing passage, in FIG. 2D, or anywhere else in Boyd that discloses or suggests that the rate of removal of the silicide layer is higher than the rate of removal of the polysilicon layer.

Thomas is not understood to disclose or to suggest anything that would remedy the foregoing deficiencies of Boyd with respect to selecting chemical mechanical polishing parameters to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate.

Although in paragraph 5, Thomas discloses that it is desirable for the removal rates of layers to differ significantly from each other in order to induce planarity and maintain the

integrity of the semiconductor substrate during polishing, Thomas neither discloses nor suggests the desirability of removing a silicide layer at a first rate and removing a polysilicon layer at a second rate where the first rate is higher than the second rate. Furthermore, Thomas' description in paragraph 10 of the types layers of a semiconductor substrate for which different removal rates may be selected does not include silicide or polysilicon. The description in paragraph 10 is produced below:

> [0010] The method of this invention is applicable to any semiconductor substrate containing: a conductive metal (such as Cu, Al, W, Pt, Pd, Au, or Ir), a barrier or liner layer (such as Ta, TaN, Ti, or TiN), and an underlying dielectric layer (such as SiO.sub.2, TEOS, PSG, BPSG, or any low-k dielectric).

There is nothing in the foregoing passage or anywhere else in Thomas that discloses or suggests selecting chemical mechanical polishing parameters to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate. Therefore, even if the teachings of Boyd and Thomas were combinable, which Applicants do not concede, their combination would fail to disclose the features of claim1.

The applied art is also not understood to disclose or to suggest the foregoing features of claims 15, particularly with respect to removing the portion of the metal silicide by chemical mechanical polishing, wherein the metal silicide is removed by chemical mechanical polishing at a first polishing rate, the portion of the dielectric layer is removed at a second polishing rate, and the first polishing rate is higher than the second polishing rate. The applied art is also not understood to disclose or to suggest the foregoing features of claims 20, particularly with respect

to selecting chemical mechanical polishing parameters to remove the metal silicide at a first rate, and to remove the material at a second rate, where the first rate is higher than the second rate.

There is nothing in Buynoski that remedies the foregoing deficiencies of Boyd and Thomas with respect to claims 1, 15, and 20. Accordingly, for at least the foregoing reasons, claims 1, 15, and 20 are believed to distinguish over Boyd, Thomas, and Buynoski.

Each of the dependent claims is also believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim and, as such, has not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claims, except as specifically stated in this paper, and the amendment of any claims does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney can be reached at the address shown below. All telephone calls should be directed to the undersigned at 617-521-7896.

Enclosed a $120.00 check for a one-month Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050 referencing Attorney Docket No. 10559-584002.

Respectfully submitted,

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